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Monte Carlo Simulation of Electron and Proton Irradiation of Carbon Nanotube and Graphene Transistors

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Abstract

Carbon-based nanotechnology electronics can provide high performance, low-power and low-weight solutions, which are very suitable for innovative aerospace applications. However, its application in the space environment where there is a radiation hazard, requires an assessment of the response of such electronic products to the background irradiance. To explore the potential of carbon-based nanotechnology, Monte Carlo simulations of radiation interacting with a gate-all-around carbon nanotube (GAA-CNFET) and a top-gated graphene FET are presented. Geant4 is used to calculate the energy deposited into the dielectric layers and the displacement damage in the nano-semiconductors under proton and electron irradiation. Both an unshielded and two cases with 250 μm thick NiFe and Pb shielding are tested at a fluence of 10^{15} m^{-2} . The energy range of the particles considered is $10^{-2} - 10^2 \text{ MeV}$ for the unshielded and $1 - 10^3 \text{ MeV}$ for the shielded case. The results indicate that the graphene transistor is more susceptible to displacement damage than the CNT-based system.

Keywords

Space Electronics; Graphene; Carbon Nanotubes; Transistors; Radiation Damage; Radiation Hardening

Introduction

Electronic components exposed to radiation lose their reliability as their function is disrupted by penetrating particles and waves. Radiation effects in silicon-based devices have been studied extensively in the past (Dressendorfer, 1998; Messenger, 1992). The emergence of post-Si electronic technologies makes it necessary for further studies of their response under equivalent conditions. Carbon-based devices are currently considered very promising future technology as they provide the highest level of

miniaturization reported until now. With the advent of new manufacturing techniques and solutions to the problems of incorporating graphitic nanostructures into electronic components, it is expected that carbon-based technology will be very common in the near future.

The idea of using electron beam irradiation to control the exact structure of carbon nanotubes (CNTs) has led to numerous microscopical studies of displacement damage for both CNTs and graphene (Tolvanen, Kotakoski, Krasheninnikov, 2007; Banhart, 1999; Smith, Luzzi, 2001; Krasheninnikov, Banhart, Li, Foster, Nieminen, 2005). This research utilizes a computational method to investigate the effect of radiation on complete electronic components incorporating such structures. Using Geant4, a Monte Carlo simulator for the passage of particles through matter, a gate-all-around CNT FET (GAA-CNFET) and a graphene FET (GFET) were constructed and exposed to proton and electron irradiation. The ionization of the dielectric layers of the two transistors as well as displacement damage of the carbon-based semiconductors were assessed.

Trapped charge in dielectrics can result in voltage shifts. In thin oxides, such as those included in this study, electron tunneling can also have a significant impact on transistor performance. Furthermore, quantum confined semiconductor nanostructures like CNTs and graphene are prone to displacement damage effects resulting from collisions with the incoming particles. Since most of the properties of such structures depend on their exact atomic arrangements, dislocating atoms from their position can alter their behavior. In CNTs, changes in the band-

gap and conductivity of the tube are reported, while in graphene further localized states near the Fermi energy and the opening of a band-gap are possible (Teweldebrhan, Balandina, 2009).

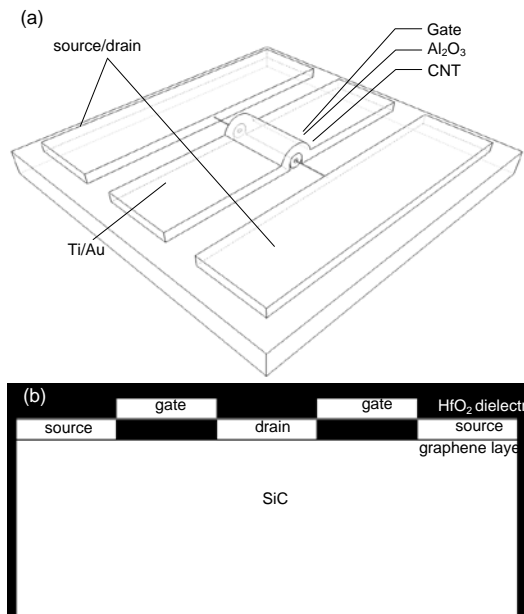


FIG. 1 SCHEMATIC 3-D REPRESENTATION OF (a) THE GAA-CNFET CREATED WITH GEANT4 AND (b) CROSS-SECTIONAL VIEW OF THE GFET

Simulation Models

The GAA-CNFET 3-D model created with Geant4 (Fig. 1a) is based on (Chen, Farmer, Xu, Gordon, Avouris, Appenzeller, 2008) and includes a Single Wall Carbon Nanotube (SWNT) with a diameter of 2 nm and density of 1.34 g/cm³ attached to palladium source and drain contacts. The tungsten nitride gate wraps around the tube and is insulated with a 7-nm-thick layer of Al₂O₃. The Ti/Au electrode is deposited above the gate and expands throughout the z-dimension of the device. Although this configuration includes a single gate, multiple gates can be supported under the same electrode. A second dielectric layer of SiO₂ with dimensions $(x=1.2) \times (y=0.1) \times (z=1)$ μm , where y is the thickness, insulates the Si substrate.

The second model is a graphene FET (GFET), based on the top-gated transistor described in (Lin, Dimitrakopoulos, Jenkins, Farmer, Chiu, Grill, Avouris, 2010). A SiC wafer volume of thickness 330 μm was constructed on top of which the 1-nm-thick layer of epitaxially grown graphene is placed. An Hf-based dielectric of thickness 10 nm is used for insulating the double gate. A gate length of 240 nm was chosen for this simulation. The source, drain and gate electrodes consist of Ti/Pd/Au layers of

thicknesses 1nm/20nm/40nm respectively. The 3-D geometry produced is depicted in Fig. 1b. The total surface area of the transistor is $(x=1.2) \times (z=30)$ μm^2 .

Both transistors were hit by particles originating from a rectangular plane equal to their top view dimensions and residing above them. This assured an isotropic fluence of particles arriving on their surface that was arranged to be 10^{15} m^{-2} . In the first set of simulations the particle energies were in the range of $10^{-3} - 10^3$ MeV, with no shielding protecting the devices. Two shielded cases were successively investigated; using 250 μm NiFe and Pb shielding that resided between the particle source plane and the surface of the transistors.

The sensitive volumes in both models are the dielectric layers for measuring the absorbed dose and incoming secondary particles, and the carbon nanostructures for calculating displacement damage. In order to produce non-ionizing energy loss (NIEL) results for the latter, the single scattering model was chosen for Coulombic interactions.

Ionization of Dielectrics

The total ionizing dose (TID) results for the three dielectric layers residing in both transistors for the unshielded case are shown in Fig. 2a. Due to the small geometry of both transistors, virtually no secondary particles were observed. Furthermore, the energy transferred from the primary particles is higher for lower kinetic energies, which produced a Bragg-like curve of ionization. Finally, protons appear more ionizing due to their higher cross-sections.

The small dimensions of the volumes contributed to remarkably high values of TID compared to those observed in conventional Si technology oxides. The absorbed energy reported in eV was, therefore, considered more appropriate (Fig. 2b). For example, the highest TID values (up to 6×10^5 Gy at 0.75 MeV) appear in the Al₂O₃ layer of the GAA-CNFET since it is the smallest of the volumes, but the highest absorbed energy appears at the HfO₂ of the GFET, as a result of its large surface.

During ion bombardment, tunneling of charge residing at an approximate distance of 5 nm from the interface with the semiconductor can constrain accumulation of trapped charge in thin dielectric layers (Schrimpf, Fleetwood, Alles, Reed, Lucovsky, Pantelides, 2011). Consequently, when examining the effects of ionization, the TID of the SiO₂ layer in the GAA-CNFET is thought to be more significant than

that of its 7-nm-thick Al_2O_3 layer. Equivalently, the 10-nm-thick HfO_2 layer in the GFET can theoretically allow for increased electron tunneling to occur. Experimental studies of the relationship between voltage shift and dielectric thickness for various materials can reveal more details about the susceptibility of the nanotransistors to ionizing radiation.

Generally, the GAA-CNFET presented in (Chen, Farmer, Xu, Gordon, Avouris, Appenzeller, 2008) suffers from trapped charge imposed during manufacturing. The final transistors derived from CNT semiconductor nanostructures might have a completely different architecture.

In Fig. 3, a thin shielding film is added between the radiation source and the transistors. Electrons were significantly absorbed only by the NiFe alloy, at energies below 20 MeV. The production of gamma rays, however, which reached up to 15% of the primary particle fluence at energies 700 – 1000 MeV, added to the energy deposited at penetrating values. Lead shielding produced minimal secondary radiation but also presented limited capability to absorb electrons at this thickness. Proton irradiation, being more penetrating, arrived at the dielectrics almost unimpeded. The energy absorbed in this case approximates that observed during the simulations where no shielding was applied.

Displacement Damage

When examining displacement effects in semiconductors, neutrons are generally considered the most prominent source of damage as, due to their lack of charge, they do not interact electromagnetically with matter. The low atomic weight of carbon, however, makes it susceptible to electron irradiation. In fact, the small cross-sections of neutrons indicate reduced possibilities of collisions with the ultra-thin layers of the quantum confined nanostructures. Unfortunately, there is a lack of information concerning neutron irradiation that is primarily a result of the extensive use of electron microscopy techniques used for examining carbon nanotubes and graphene. Since electron irradiation is most widely studied, only electron-induced displacement damage was considered in this work.

To statistically measure displacement damage in the two nano-semiconductors, the NIEL functionality of Geant4 was used. The latter allows the computation of the energy deposited in a material that does not contribute to ionization. It is known from the literature

(Smith, Luzzi, 2001) that the energy of an incoming electron colliding with a carbon atom in CNTs and graphene must be approximately 86 keV or higher in order for the atom to be displaced and to not be instantaneously recombined. During simulations, the incoming electrons, which produced NIEL and whose energies were above the displacement energy threshold were measured. The results for the unshielded case are shown in Fig. 4.

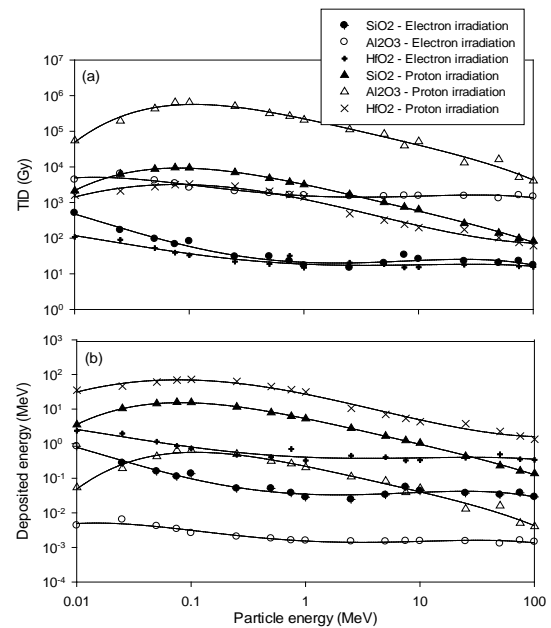


FIG. 2 TID AND ABSORBED ENERGY IN THE DIELECTRIC LAYERS, FLUENCE = 10^{15} m^{-2}

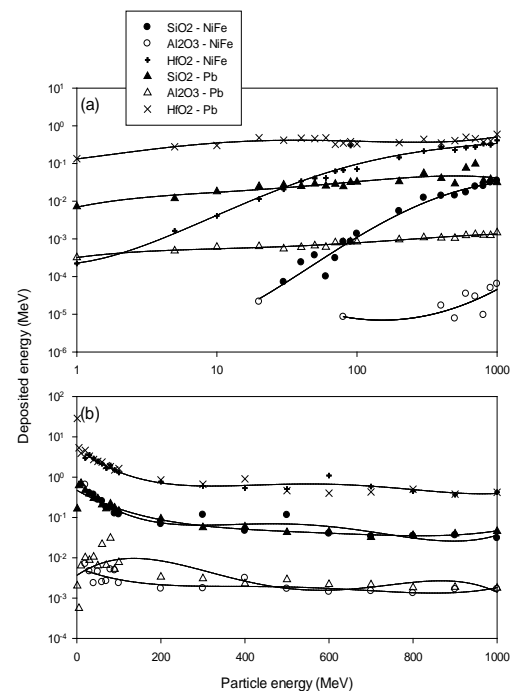


FIG. 3 ENERGY ABSORBED BY THE DIELECTRICS WITH NiFe AND Pb SHIELDING OF THICKNESS $250 \mu\text{m}$ DURING ELECTRON (a) AND PROTON (b) IRRADIATION, FLUENCE = 10^{15} m^{-2}

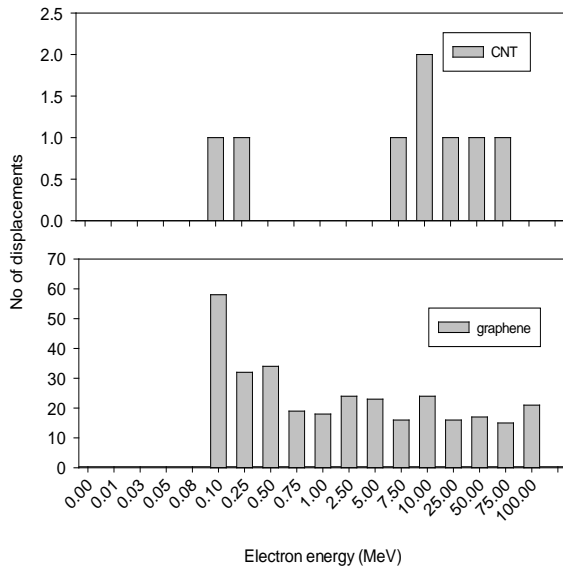


FIG. 4 DISPLACEMENT DAMAGE FOR THE UNSHIELDED CNT AND GRAPHENE, FLUENCE = 10^{15} m^{-2}

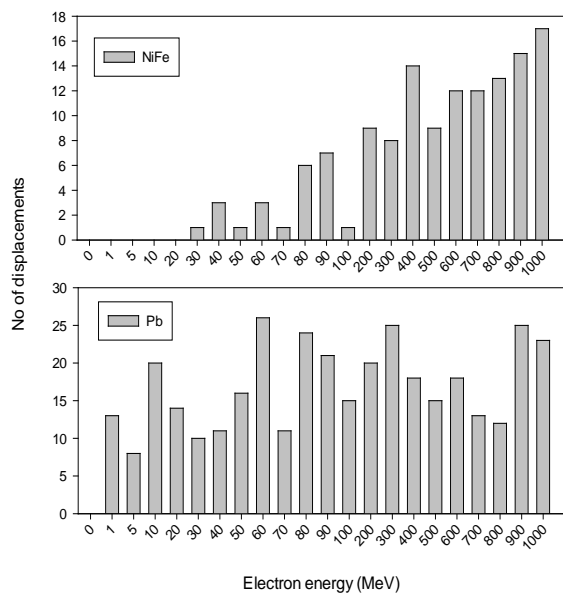


FIG. 5 DISPLACEMENT DAMAGE FOR THE GRAPHENE LAYER WITH NiFe AND Pb SHIELDING APPLIED.

It is evident that the large surface area of graphene resulted in increased interactions with the incoming particles. On the contrary, the CNT shows a high degree of hardness to displacement damage as a result of its thin tubular geometry. With the addition of Pb shielding, CNT damage reduced even further and, using NiFe shielding, it appeared to be completely eliminated. Displacement damage results for graphene for the shielded case are shown in Fig. 5. NIEL-induced damage appears relatively reduced only at the lower values of the energy range. To block higher

energy particles a greater shielding thicknesses must be considered.

When combined with existing theoretical models of subsequent changes in electrical properties of the nanostructures as a result of irradiation, displacement damage measurements facilitate estimation of the final effects on transistor operation. Such effects can include increased resistivity and changes in current gain.

Conclusions

Simulation results of irradiation of a GAA-CNFET and a graphene FET have been presented. Ionization of the dielectric layers appeared increased in the unshielded case of electron irradiation for lower energies, but with proper shielding significant reduction can be achieved. Further studies on electron tunneling through the oxides can reveal the degree of susceptibility of the devices to charge-induced voltage shifts. Displacement damage proved more important for the GFET due to its large surface area placed orthogonal to the particle stream.

The results presented herein were produced using the current standard mathematical models of Geant4. Further revision of the models for very thin layers and quantum confined nanostructures will lead to more accurate estimation that is suitable for future technology developments.

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